(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 951 068 A1

# (12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
**20.10.1999 Bulletin 1999/42**

(51) Int. Cl.[6]: **H01L 23/10**, G01L 9/00

(21) Application number: **98870132.2**

(22) Date of filing: **10.06.1998**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE**
Designated Extension States:
**AL LT LV MK RO SI**

(30) Priority: **17.04.1998 EP 98870085**

(71) Applicants:
- **INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW**
  **3001 Heverlee (BE)**
- **C.P. Clare Corp.**
  **Beverly, MA 01915-1048 (US)**

(72) Inventors:
- **Tilmans, Hendrikus A.C.**
  **6229 XA Maastricht (NL)**
- **Beyne, Eric**
  **3001 Leuven (BE)**
- **Van De Peer, Myriam D.J.**
  **1090 Brussels (BE)**

(74) Representative:
**Van Malderen, Joelle et al**
**Office Van Malderen,**
**Place Reine Fabiola 6/1**
**1083 Bruxelles (BE)**

## (54) Method of fabrication of a microstructure having an inside cavity

(57) The present invention relates to a method of fabricating a microstructure having an inside cavity comprising the steps of:

- depositing a first layer or a first stack of layers in a substantially closed geometric configuration on a first substrate;
- performing an indent on the first layer or on the top layer of said first stack of layers;
- depositing a second layer or a second stack of layers substantially with said substantially closed geometric configuration on a second substrate;
- aligning and bonding said first substrate on said second substrate such that a microstructure having a cavity is formed according to said closed geometry configuration.

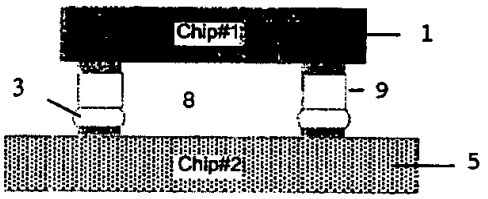



FIG. 8



EP 0 951 068 A1

## Description

### Object of the invention

[0001] The present invention is related to a method of fabrication of a microstructure having an inside and preferably a sealed cavity.

[0002] The present invention is also related to the product obtained by said method, which is related to a microstructure having a sealed cavity.

### State of the art

[0003] Microstructures with a cavity can be formed by making an assembly of two ships or two wafers or a chip-on-wafer with a spacer in-between. Such structures should have hermetically sealed cavities with a controlled ambient (gas composition and/or pressure).

[0004] These structures can be used for a lot of different applications such as microaccelerometers, microgyroscopes, microtubes, vibration microsensors, micromirrors, micromechanical resonators or "resonant strain gauges", micromechanical filters, microswitches and microrelays.

[0005] Traditionally, for these applications, the ambient of the cavity is defined during the assembly of the several components by anodic, fusion or eutectic wafer bonding, wafer bonding using low temperature glasses or polymers as the brazing material, reactive sealing techniques, etc.

[0006] The document US-5296408 is describing a fabrication method for a microstructure having a vacuum sealed cavity therein including the process steps for the formation of an aluminum filled cavity in a body of silicon material and heating the structure such that the aluminum is absorbed into the silicon material leaving a vacuum in the cavity. In one embodiment, a cavity is etched into a silicon wafer and filled with aluminum. A silicon dioxide layer is formed over the aluminum filled cavity and the structure is heated to produce the vacuum cavity.

[0007] The document "*Fluxless flip-chip technology*" of Patrice Caillat and Gerard Nicolas of LETI, published at the First International Flip-Chip Symposium, San Jose, California, February 1994 describes a flip-chip assembly of two chips with a solder sealing ring defining a cavity during the assembly itself. The assembly and the subsequent sealing are normally done in air or under an $N_2$ purge. Similar conditions may exists for the other wafer bonding techniques as mentioned hereabove (except for the technique of reactive sealing). However, anodic or fusion bonding techniques as well as the techniques using low temperature glasses or polymers for the bond can also be accommodated such that a better control over the ambient as compared to the method described by Caillat, et al. is achieved.

[0008] However, wafer bonding techniques such as anodic bonding and silicon fusion bonding require a very clean, i.e., low particle count, environment. Bonding techniques based on a solder bond, on the other hand, are less susceptible to particles. Furthermore, flip-chip solder bonds also have the interesting property of self-alignment (within certain limits) and display a good control, predictability and reproducibility of the solder height and thus the cavity height. Furthermore, a solder bond leads to a metallic seal, which is known to provide the best hermeticity possible. Also, the metallic seal can be used as an electrical feedthrough from one chip (e.g. the bottom chip) to the other (e.g. the top chip of the stack).

### Aims of the present invention

[0009] The present invention aims to suggest a method of fabrication of a microstructure having an inside cavity. More particularly, the present invention aims to suggest to have a sealed cavity with a controlled ambient allowing a free choice of the sealing gas composition and the sealing pressure or a vacuum.

[0010] Another aim of the present invention is to suggest a method which does not require special equipment to perform the fabrication of such microstructures in a vacuum or controlled inert gas ambient.

### Main characteristics of the present invention

[0011] The present invention is related to a method of fabrication of a microstructure having an inside cavity comprising the following steps:

- making a first layer or a first stack of layers in a substantially closed geometric configuration on a first substrate;
- performing an indent on the first layer or on the top layer of said first stack of layers;
- making a second layer or a second stack of layers substantially with said substantially closed geometric configuration on a second substrate;
- aligning and bonding said first substrate on said second substrate such that a microstructure having an inside cavity is formed according to said closed geometry configuration.

[0012] An indent can be defined as a groove made in a layer such that when the two substrates are bound, a connection, preferably a contacting channel, between the inside cavity of a microstructure and the outside ambient is performed.

[0013] Such indent can be performed using lithographic/chemical steps or by mechanically removing a part of the first layer using a shearing tool or by applying a force using an indent tool on the first layer.

[0014] By making a layer on a substrate, it is meant depositing or growing a layer on such substrate.

[0015] Thereafter, the indent is closed by reflowing said first layer at a reflow temperature above the melting

temperature of said first layer. By reflow temperature, it should be understood the temperature at which said first layer is fusible but not the substrate and/or the structure materials thereon.

**[0016]** Further characteristics or advantages will be found in the following description of several preferred embodiments of the present invention.

## Brief description of the drawings

**[0017]**

Figures 1 to 6 represent the several steps of a preferred embodiment of the method of fabrication of a microstructure having a sealed cavity according to the present invention.

Figures 7 and 8 represent the two last steps of a second preferred embodiment of fabrication of a microstructure having a sealed cavity according to the present invention.

Figures 9 to 11 represent in detail three possible method in order to create the indent necessary to achieve the method of fabrication of microstructure having a sealed cavity according to the present invention.

Figures 12 to 15 represent several possibilities of applications of microstructure fabricated according to the method of the present invention.

## Detailed description of preferred embodiments of the present invention

**[0018]** The present invention will be described more in detail hereunder referring to specific embodiments which are more precisely described in the drawings.

**[0019]** The method of fabrication of a microstructure having a sealed cavity, according to the present invention can be recalled as indent-reflow-sealing (IRS) technique, which is based on a flip-chip technique using a fluxless soldering process, and which allows to make hermetically sealed cavities with a controlled ambient (gas(es) and pressure) preferably at low temperature (typically of the order of 300°C).

**[0020]** By controlled ambient, it should be understood that the inside ambient in the cavity is not in direct contact with the outside ambient. The pressure (or vacuum) in the cavity as well as its gas composition can therefore be adapted to the user requirements .

**[0021]** The cavities are formed by making an assembly of two chips (or two wafers, or chip-on-wafer) with a spacer in between. The spacer typically consists of a solder layer with or without an additional spacer layer. The alignment is done as a pick&place operation (in particular applicable for chip-on-wafer processes) on a flip-chip aligner/bonder. An important characteristic of the present invention is that the sealing is done in an oven as a post-assembly operation, i.e., not during the assembly operation itself. The fact that the cavity sealing is done in an oven makes the present method more flexible with respect to the choice of the sealing gas and the sealing pressure. Standard flip-chip assembly as used by Caillat, et al on the other hand, is done in air ambient, with or without a nitrogen flow over the devices.

**[0022]** From a manufacturing standpoint, it should be noted that the IRS technique according to the present invention has a cost advantage as compared to the other methods of the state of the art. The pick&place operation done on the flip-chip aligner&bonder is in general the most time-consuming and most expensive step. By doing the reflow operation as a post-assembly step in an oven, the operate time on the flip-chip aligner is (drastically) reduced. In addition, large batches of chip-on-wafer (or chip-on-chip) assemblies can be sealed in an oven at the same time. All this results in a high throughput and reduction in manufacturing costs.

**[0023]** A specific embodiment of the method of fabrication of a microstructure according to the present invention, which is based on the assembly chip-on-chip will be described hereunder in reference with figures 1 to 6, wherein an explanation of the different processing steps follows hereunder:

**Step 1**: Preparation of the first chip (figure 1)

**[0024]**

- deposition and patterning of a metallization seed layer (2) on the first chip (1),
- preparation of a plating mould (e.g., polyimide which can be as thick as 100 μm) and electrodeposition (electroplating) of the solder (3). Some examples of possible solders can be SnPb63/37, SnPb5/95, SnPbAg (2% Ag), In, AuSn (80/20), SnAg, SnAgCu, SnBi, etc.
- removing the mould and making the indent or groove (4). This can also be conveniently done on wafer level, the wafer is next diced to obtain the individual chips.

**[0025]** Advantages of using a solder in the present method of the invention are as follows:

- the solder is of a soft material, thus allowing making an indent using a shearing tool or an indenting tool (soft should be understood as opposed to brittle, hard,...). The indent can be made in a photolithographic/chemical way, or, through mechanical means.
- the solder can be reflowed at moderate temperatures (200-350°C) below than the melting point of the substrate. Due to the high surface tension, the indent will completely disappear after reflow (the solder is brought back into its shape without any traces of the indent);
- the solder can be electroplated using LIGA-like

processing. It is thus convenient to define a geometrically enclosed structure forming an inside sealed cavity afterwards. In addition, electrodeposition allows the fabrication of high cavity walls (> 5 µm). This facilitates the making of the indent as well.

- the solder leads to an excellent hermetic seal of the cavity.

**Step 2** : Preparation of the second chip (figure 2)

**[0026]**

- deposition and patterning of suitable metallization layer (6) on the second chip (5) (this can also be conveniently done on wafer level). The requirements for a suitable metallization layer should be a good wettability and the formation of stable intermetallic compound with solder (3). For instance, if a SnPb-base solder is used in Step 1, most stable SnCu will be convenient. A seed layer of SnNi can also be used. Therefore, the SnNi layer needs also to be covered by a thin Au layer since Ni oxidises in air. A thickness of the Au layer will be in the range of 0.1 - 0.3 µm for having a good wettability while having a thicker Au layer will result in an unreliable solder connection. If a AuSn-base solder will be used, a Au metallization will yield good results. This metallization will serve as the counter metallization for the flip-chip operation (see step 3).

**Step 3 :** Pre-treatment "flip-chip" alignement (figure 3)

**[0027]**

- On flip-chip aligner & bonding device, both chips (1 & 5) are aligned so that the solder ring (3) on the first chip is aligned with the metal ring (6) on second chip. Before loading, both chips are preferably given an adequate plasma pretreatment in order to achieve a reliable adhesion (s-called "pre-bond", see step 4) of both chips without solder reflow.

**Step 4** : Pre-bonding (figure 4)

**[0028]**

- Both chips are heated to a temperature well below the melting point of the solder, for instance for SnPb (67/37) having a melting point 183 °C, the chips are typically heated to a temperature comprised between 120-160°C. The chips are next prebonded by applying a bonding force (F), (typically of 2000 gf). The chips now "stick" and can be moved to the reflow oven. The exact temperature and bonding force depend on the solder, the solder history and the type of metallization used.

**Step 5** : Pump vacuum and filling of the cavity (figure 5)

**[0029]**

- In the reflow oven, the cavity (8) is evacuated and next filled with the desired gas such as $N_2$ or a gas mixture such as $N_2/H_2$ mixture or even SF6 to a required pressure. Optionally, the cavity could be left at a vacuum pressure.

**Step 6** : Reflow and sealing (figure 6)

**[0030]**

- The temperature of the oven is now raised above the melting point of the solder but below the melting point of all other materials used. The solder (3) will melt so as to close the indent resulting in a hermetically sealed cavity with a controlled ambient.

**[0031]** The process flow as represented in figs. 1 to 6 shows an assembly in which the cavity height is set by the solder itself, without using any additional spacer layer. However, the method for an assembly with an additional spacer layer could be described in reference to figure 7 and 8.

**[0032]** Figures 7 and 8 are representing the two last process steps of the method of fabrication according to the present invention using a spacer layer (9) in combination with the solder layer (3) according to said cavity height.

**[0033]** Figures 9, 10, and 11 represent in detail three methods of creating an indent in the preparation of one of the two chips.

**[0034]** More particularly, figures 9 represent a local electrodeposition of the solder using a patterned mould (comparable to LIGA as 3D-microforming techniques), wherein :

- figure 9a shows the deposition of a seed layer, the growing of the mould material (10) (e.g. photoresist, polyimide), and the patterning of the mould;
- figure 9b shows the electrodeposition of the solder (3);
- figure 9c shows the removing of the mould and seed layer (locally).

**[0035]** Figure 10 represents a second method of creating an indentation by removing the solder using a shearing tool such as a shear tester.

**[0036]** Figure 11 represents a third method of creating an indentation by using an indenter wherein the indent of the solder is made by applying a (high) force.

**[0037]** The two last embodiments represented in figures 10 and 11 are possible because the solder is a soft material that allows an indentation by forcing a tool such as a shearing or an indenting tool.

**[0038]** Figures 12 to 15 represent several structures

using the method of fabrication of a microstructure having a sealed cavity according to the present invention for specific applications such as a microreed switch (figure 12), a capacitive microaccelerator (figure 13), a vacuum microtriode (figure 14), a one-port microresonator using electrostatic drive/sense (figure 15), a microrelay (not represented).

## Claims

1. A method of fabricating a microstructure having an inside cavity comprising the steps of:
   - making at least a first layer (3) in a substantially closed geometric configuration on a first substrate (1);
   - performing an indent (4) in said first layer (3);
   - making at least a second layer (6) substantially with said substantially closed geometric configuration on a second substrate (5);
   - aligning and bonding said first substrate (1) on said second substrate (5) such that a microstructure having a cavity (8) is formed according to said closed geometry configuration.

2. The method as recited in claim 1, wherein the indent is performed using photolithographic/chemical steps.

3. The method as recited in claim 1, wherein the indent is performed by removing a part of the first layer using a shearing tool (11).

4. The method as recited in claim 1, wherein the indent is performed by applying a force to an indent tool (12) on the first layer.

5. The method as recited in any one of the preceding claims, wherein a pre-treatment prior to the aligning and bonding of said substrates is performed on both substrates, said pre-treatment consisting in a plasma etching treatment.

6. The method as recited in any one of the preceding claims, wherein a pre-bonding treatment is performed after the aligning of both substrates in order to form the microstructure.

7. Method as recited in claim 6, wherein the pre-bonding treatment consists in heating the microstructure to a softening temperature well below the melting temperature of the first layer.

8. A method as recited in any one of the preceding claims, wherein said first layer is a solder layer essentially made of PbSn.

9. A method as recited in any one of the preceding claims, the first stack of layers comprises a metallization seed layer (2).

10. A method as recited in any one of the preceding claims, further comprising the step of pumping said cavity.

11. Method as recited in claim 10, further comprising the step of filling the cavity with a gas or a gas mixture to a predetermined pressure;

12. Method as recited in 11, wherein the gas is an inert gas.

13. The method as recited in any one of the preceding claims, wherein the indent is closed by reflowing the first layer at a reflow temperature above or equal to the melting temperature.

14. The method as recited in claim 13, wherein the reflowing is performed in a vacuum environment.

15. The method as recited in claim 14, wherein the reflowing is performed in an inert gas environment.

16. The method as recited in claim 14 or 15, wherein the reflowing is performed in an environment having a temperature which is less than the melting point of the substrate and the other materials thereon.

17. Method as recited in any one of the preceding claims, wherein both substrates can be silicon or chips in silicon or wafers or one being a chip, the other a wafer.

18. Microstructure having a sealed cavity (8), wherein said cavity is defined by walls according to a closed geometric configuration between two substrates (1 and 5), said walls being a stack of layers comprising at least the first metallization layer (2), a reflowed solder layer (3), and a second metallization layer (6).

19. Use of the method as recited in any one of the preceding claims for realising a microreed switch, a capacitive microaccelerator, a vacuum microtriode, a microresonator, a microrelay and a microswitch.

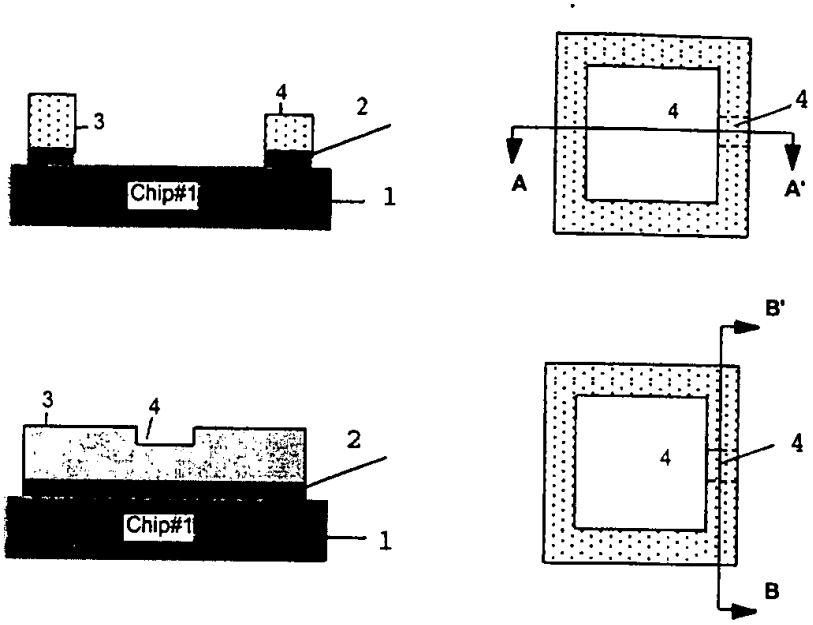



FIG. 1


FIG.2

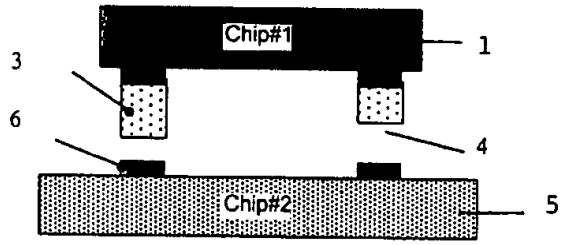



FIG.3

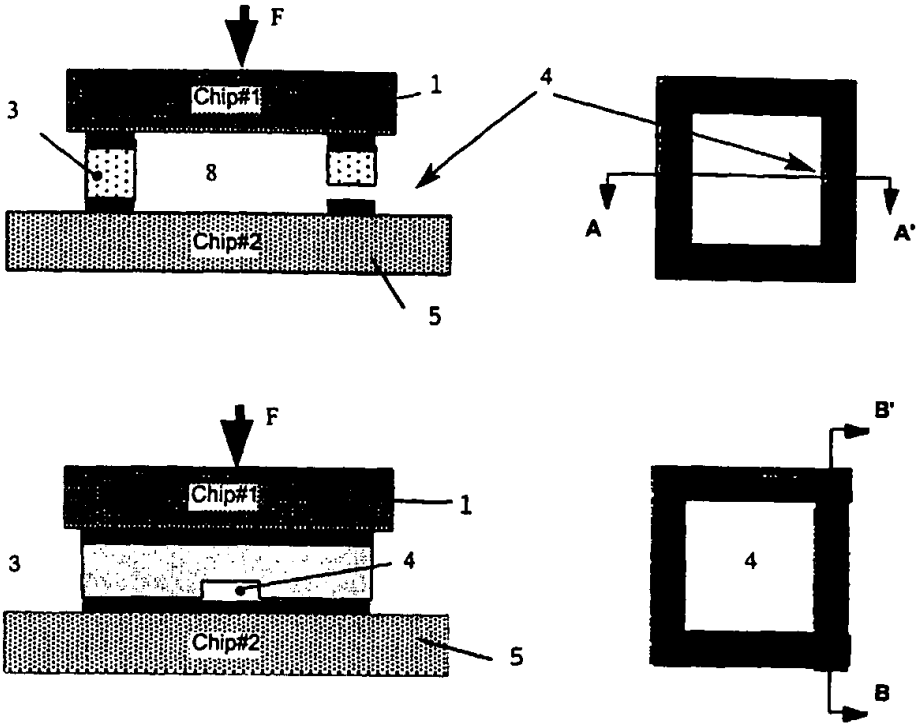



FIG. 4

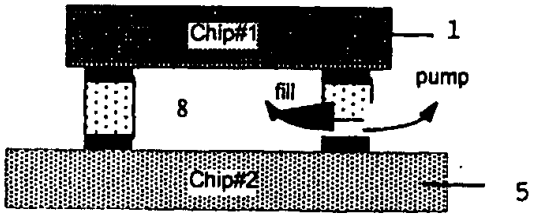



FIG. 5

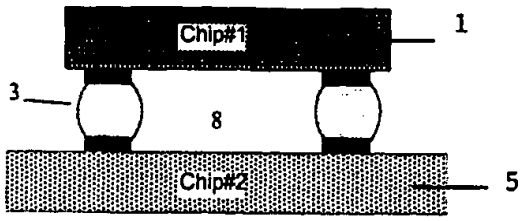



FIG. 6

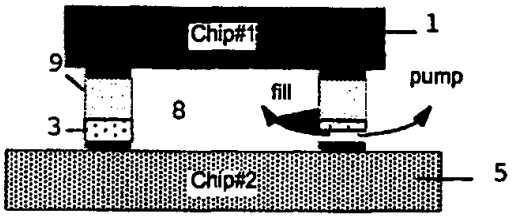



FIG. 7

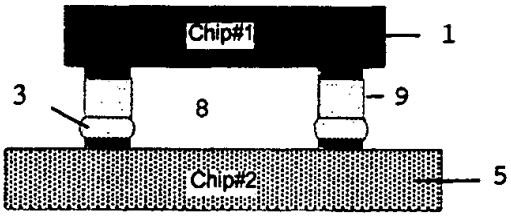



FIG. 8

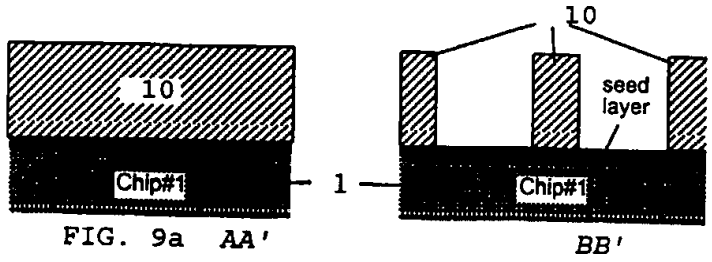



FIG. 9a AA' BB'

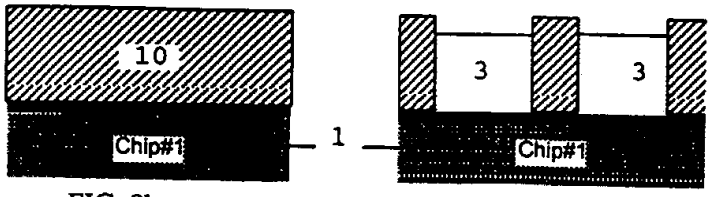



FIG. 9b

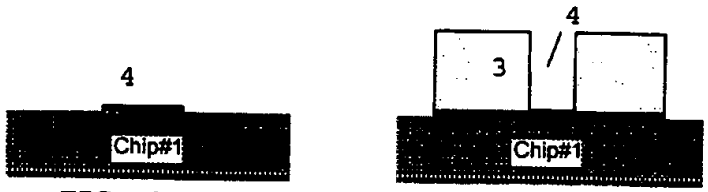



FIG. 9c

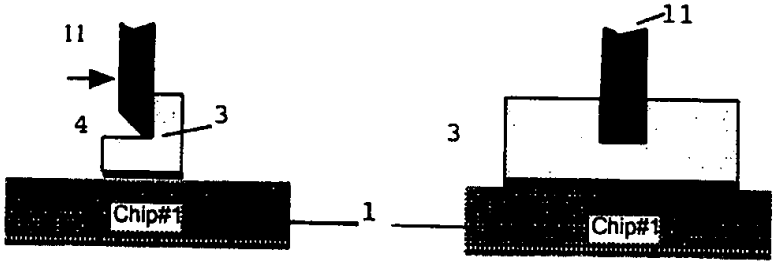



FIG. 10

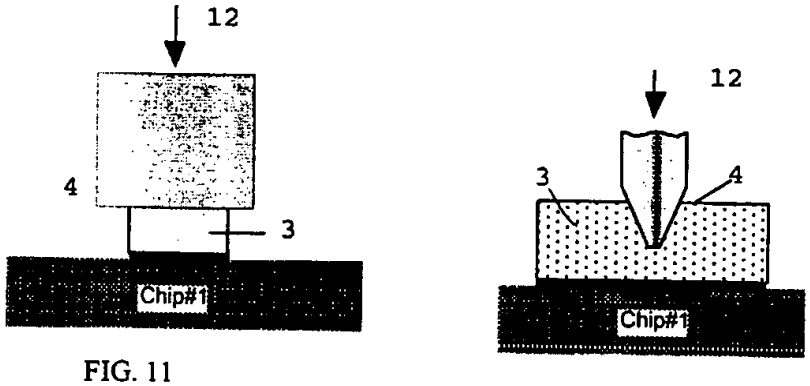



FIG. 11

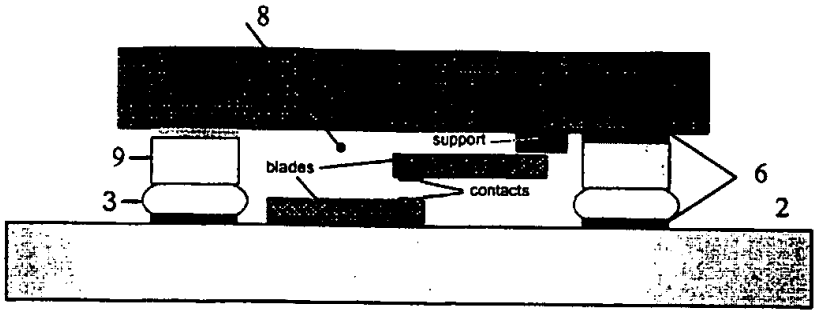



FIG. 12

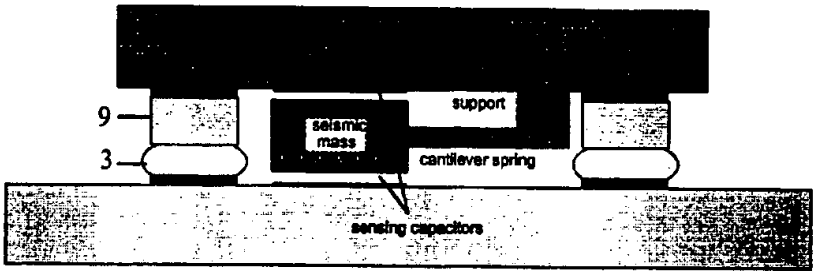



FIG. 13

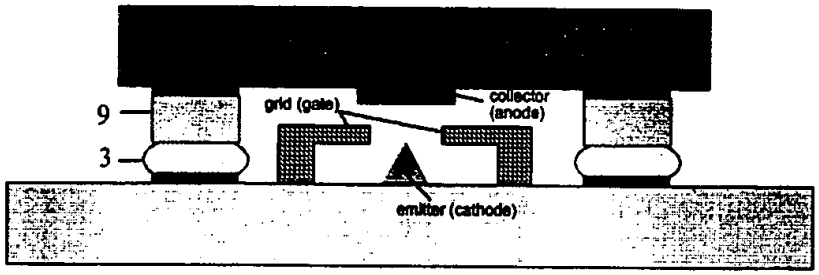



FIG.14

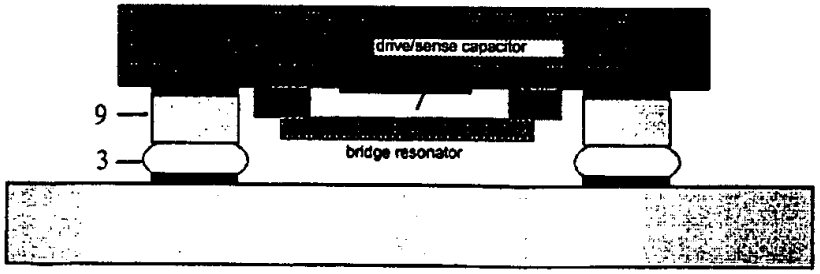



FIG. 15

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 98 87 0132

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| E | EP 0 849 578 A (MURATA MANUFACTURING CO) 24 June 1998<br>* the whole document * | 1,2,9, 10,13, 14,16-19 | H01L23/10<br>G01L9/00 |
| X | US 5 317 922 A (BOMBACK JOHN L ET AL) 7 June 1994 | 18,19 | |
| A | * the whole document * | 1,2,5,6, 8-10,13, 14,16,17 | |
| X | WO 98 05935 A (INTEGRATED SENSING SYSTEMS INC) 12 February 1998 | 18,19 | |
| A | * the whole document * | 1,11,15, 17 | |
| A | US 5 335 550 A (SATOU KIMITOSHI) 9 August 1994<br>* column 6, line 9 - column 7, line 20; figures 1-12 * | 1,2,10, 14 | |
| A | PATENT ABSTRACTS OF JAPAN vol. 006, no. 175 (P-141), 9 September 1982 & JP 57 093225 A (MITSUBISHI ELECTRIC CORP), 10 June 1982<br>* abstract * | 1,10,13, 14,16,17 | TECHNICAL FIELDS SEARCHED (Int.Cl.6)<br>H01L<br>G01L<br>B81B |
| D,A | US 5 296 408 A (WILBARG ROBERT R ET AL) 22 March 1994<br>* the whole document * | 1,18,19 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 31 May 1999 | Brock, T |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 98 87 0132

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

31-05-1999

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| EP 0849578 A | 24-06-1998 | JP 10189795 A | 21-07-1998 |
| US 5317922 A | 07-06-1994 | NONE | |
| WO 9805935 A | 12-02-1998 | AU 4053697 A | 25-02-1998 |
| US 5335550 A | 09-08-1994 | JP 2729005 B | 18-03-1998 |
| | | JP 5283712 A | 29-10-1993 |
| | | DE 4223455 A | 07-10-1993 |
| US 5296408 A | 22-03-1994 | EP 0604342 A | 29-06-1994 |
| | | JP 2077734 C | 09-08-1996 |
| | | JP 6232020 A | 19-08-1994 |
| | | JP 7105318 B | 13-11-1995 |

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭59—88864

| ⑤1Int. Cl.³ | 識別記号 | 庁内整理番号 | ⑬公開　昭和59年(1984)5月22日 |
|---|---|---|---|
| H 01 L 23/48 | | 6819—5F | |
| 25/00 | | 7638—5F | |

発明の数　1
審査請求　未請求

（全 5 頁）

# ⑤4半導体装置の製造方法

⑳特　　願　昭57—199207
㉒出　　願　昭57(1982)11月12日
⑦2発 明 者　近藤修司
門真市大字門真1006番地松下電器産業株式会社内
⑦2発 明 者　白ケ澤強
門真市大字門真1006番地松下電器産業株式会社内
⑦1出 願 人　松下電器産業株式会社
門真市大字門真1006番地
⑦4代 理 人　弁理士　中尾敏男　　外1名

2 ページ

明　　細　　書

1、発明の名称

半導体装置の製造法

2、特許請求の範囲

(1) 半導体装置の機能素子をその主面中央部に構成した半導体主基板上に、少なくとも2辺が該主基板寸法より小さい機能素子をその主面中央部に構成した半導体従基板の主面を対向載置せしめ、前記主基板と従基板を電気的，物理的に結合させる構造の半導体装置において、前記電気的結合を半田合金等のバンプ或はペデスタルで結合させると共に、該半導体基板の機能素子領域をその内側に取囲む形状に構成した半田合金等の周壁を、主基板と従基板を上の機能素子領域を気密封止結合せしめた半導体装置の製造法。

(2) 従基板を、金属薄板或はセラミック薄板とし、同薄板と主基板を気密封止結合させることを特徴とした特許請求の範囲第1項記載の半導体装置の製造法。

3、発明の詳細な説明

産業上の利用分野

本発明はＩＣ．ＬＳＩ等の半導体集積回路の製造法に関するものであり、特に高集積度、高密度実装技術を提供するものである。

従来例の構成とその問題点

システム機器の小型化，高密度化の要求に伴ない、その主要構成要素である半導体集積回路（以下ＬＳＩと略称する）も高集積度化，高密度化が望まれる。

これらの要望に答えるべくパッケージの小型化或は新規な高密度実装方式が種々提案されている。

その一例を第1図のフリップチップ法により説明する。

第1図に於いて、セラミック基板1の主面上には、配線パターン2及び外部電極端子3が設けてあり、更にＬＳＩチップ4の電極部（図示せず）を、同基板上の配線パターン2の所定部位に接続するための内部電極（図示せず）が配置された構成となっている。

ＬＳＩチップ4とセラミック基板1上の配線パ

ターンとの接続は、チップ或は基板上に設けた接続用電極（バンプ或はペデスタル）によりリフロー方式などで両者を直接接続する方法が用いられている。

本方法によれば、同一配線基板上に複数個のＬＳＩチップが載置出来、更にＬＳＩチップ相互間の配線が出来るため、旧来の方法に比較すると高密度なＴＳＩ実装法が実現提供することが出来る。

しかしながら本説明に示した如き実装法には以下に示す問題点を有するものである。

即ち、同一基板上に複数のＬＳＩチップを二次元的に配置するため、実装するＬＳＩチップの個数が増加するにしたがって、基板面積は増大する。

また、これらの実装を行なった基板は気密封止式はプラスチックモールド等の方法に依り、機械的強度を保持させると共にチップ表面部位に対する水分等の影響からの保護措置を講じる必要があり、特に後者の場合チップ表面保護膜、所謂パッシベーション膜の品質が、該半導体装置の信頼性の大きな影響を及ぼしている。

発明の目的

本発明は上述の諸問題について鑑みなされたものであり、ＬＳＩチップの高密度実装を実現すると共に、信頼性の高い半導体装置を提供することを目的とした半導体装置の製造法に係るものである。

発明の構成

本発明は高密度，高信頼度実装を実現する為に主ＬＳＩ基板の主面上に、該ＬＳＩ基板寸法より少なくとも２辺の寸法が小さい従基板の主面を、該ＬＳＩ基板の主面に対向させて載置し、両者電気的結合をバンプ或はペデスタルにより行なわせしめると共に主基板、及び従基板の主面に形成された機能素子領域部を包囲すべく形成した、周壁状バンプ或はペデスタルにより、主基板上に従基板を密着し、該機能素子領域部を気密封止する製造法によって得られる半導体装置である。

実施例の説明

本発明による半導体装置の製造法の実施例を第２図以下により説明する。



第２図は本発明の一例を示した半導体装置の主基板５（第２図Ａ）及び従基板６（第２図Ｂ）の主面部を示す平面略図である。

基板５及び基板６には夫夫その中央部に半導体装置としての機能素子領域７，7′を有し、その外周域には電極部８，8′が形成してあり、同電極群８，8′と機能素子領域７，7′は夫夫ＡＬ配線パターン（図示せず）により接続されている。

以上の如き基本構成を有する主基板５に対する従基板６の、電気的，物理的結合は所謂フリップチップ方式により行なう。

即ち従基板６の電極群8′に対応した位置に当る主基板５上の機能素子領域７部には、主基板５の機能素子と従基板６に構成した機能素子を電気的に結合する接続電極９を、ＡＬ或はＭｏ等の電極配線素材を用い、主基板５の機能素子構成時の配線用ホトプロセスにより同時に形成する。

次に第３図の断面略図に示す如く、主基板５の表面全域に保護膜層１０を形成し、電極パッド８及び接続電極９部の保護膜を選択的に除去し両電



極部位８，９を露出させ、しかる後接続電極部に対し接合金属層所謂ペデスタル１１を形成する。同ペデスタルの形成，構造は第４図に示す如く、まづ、電極金属材料（例へばＡＬ）と保護膜材料（例へば$SiO_2$）の接着力の高い接着層１２を、Ti，Cr，NiCr 等の金属により形成し、次に同層上に対し接合金属とＡＬ等の電極材料との反応を抑制するバリア金属層１３をPt，Pb，Ni，Rh，Cu 等の金属を用いて積層し、しかる後ペデスタル材であるSn−Pb，Sn−Ag等からなる半田合金に依りなるペデスタル１１を同層上に１０μm ～数10μm の高さで形成する。

この時、従基板６の電極8′部に対しても、同様に接着層金属１２及びバリア金属層１３を積層形成する。なお、接合金属ペデスタルは上記例では主基板５上に設けた例で説明したが、従基板６上に接合金属層を構成した所謂バンプを設ける方式であっても何ら支障はない。

上記接合電極金属層であるペデスタル或はバンプ形成時に、第２図Ａ，Ｂ及び第３図～第５図に

7 ページ

示す如く、主基板５の接続電極パッド９群の外周域でかつ従基板６の電極パッド９群と同基板の周縁部の間の領域に、機能素子領域７，7′部を包囲する形状の封止金属壁１４を同時に形成する。

即ち、主基板５上にペデスタルを構成する構造の場合には、第３図，第４図の様に接続電極パッド９上に接着層金属１２及びバリア金属１３を形成すると共に、封止金属層１４形成部位に対しても同様に上記金属層１２，１３を形成し、ペデスタル９形成時においては、同部位には半田金属による封止金属層１４を同時に形成するものである。

なお同領域は通常絶縁膜である保護膜１０上に形成するため、ペデスタル（或はバンプ）金層と下地金属の反応を抑制する目的のバリア金属層13の存在は必要としないが、ペデスタル（或はバンプ）形成プロセスと同時に形成する関係上同領域に対してもバリア金属層１３が形成されている。

以上の如く、ペデスタル或はバンプの形成と同時に、同一素材からなる封止金属層１４を有する、主基板５と従基板６を、通常のフリップチッププロセスにより、第６図の如く主基板５上に従基板６を所定の位置に設置した後、半田リフロー処理を施こせば、主基板５上の機能素子と従基板６上の機能素子は電気的に結合されると共に、封止金属層１４により主基板５と従基板６は従基板６の周縁域全面に亘り結合され、夫夫の基板上に構成してある機能素子領域７，7′は同封止金属層１４により外気より気密封止がなされる。

しかる後主基板５の周辺部に設けた電極８を、パッケージのリード電極とワイヤ接続し、プラスチックパッケージで封止を行ない半導体装置を完成させる。

なお本発明の上記実施例では主基板及び従基板共に機能素子を構成し、実装密度を高めると共に機能素子部の気密封止を行なう製造法により説明したが、実装密度の向上に対する要望が比較的少ない場合には、機能素子は主基板上にのみ構成し、従基板は、金属薄板或はセラミック薄板を用いて該機能素子部を気密封止する製造法を採用することも出来る。

9 ページ

発明の効果

本発明は実施例において記載した如く、機能素子を有する主基板の主面上に、他の機能素子を有する従基板を近接対向装置し両者を電気的，物理的に結合させているため高集積度，高密度の実装が可能となり小型化実装法を容易に提供するものである。

また、上記両者の物理的結合が機能素子領域の周囲全域で形成しているため、機能素子領域は気密封止構造となり、同領域への水分等の侵入が阻止され信頼性の高い半導体装置となすことが出来る。

よって、外囲器を例へばフィルムキャリア方法等の小型実装を用いる場合においても、外囲器は電極リードと物理的，機械的強度を保持する機能のみを有すれば良く、同外囲器による対耐湿性機能が不用となり、その構造を簡単なものとなることが出来、小型化の推進に寄与することが大きい。

4、図面の簡単な説明

第１図は従来のフリップチップ方式を示す平面

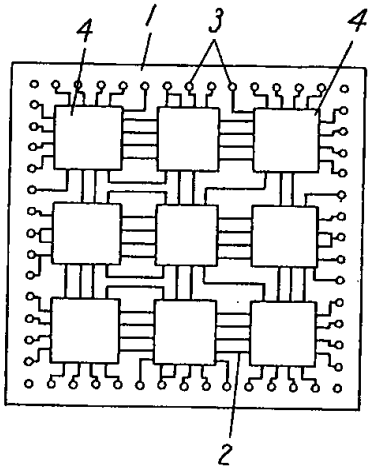
10 ページ

図、第２図Ａは本発明の実装例を示す主基板の平面図、第２図Ｂは本発明の実施例を示す従基板（第２図Ｂ）の平面図、第３図は同主基板の断面図、第４図は同拡大図、第５図は従基板の断面図、第６図は本発明により構成した半導体装置の断面図である。

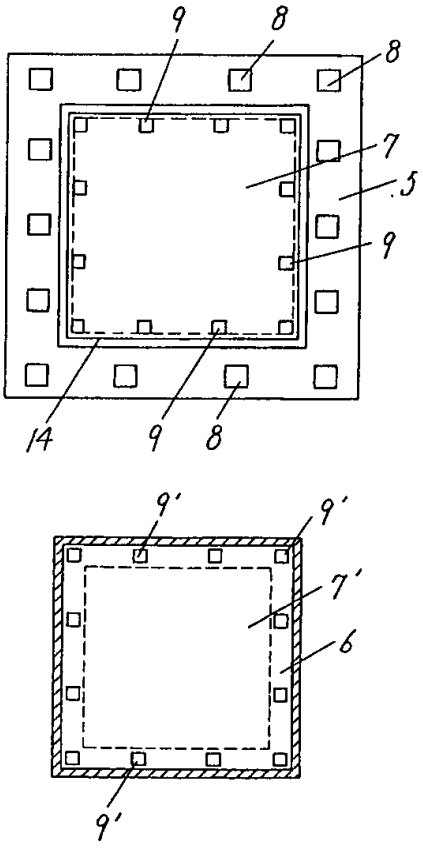
５……主基板、６……従基板、７，7′……半導体装置の機能素子領域、８……外部引出電極図パッド、９……接続電極パッド、9′……従基板上の接続電極パッド、１０……パッシベーション膜、１１……接合金属層、１２……接着層金属層、13……バリア金属層、１４……封止金属層。

代理人の氏名　弁理士　中　尾　敏　男　ほか１名

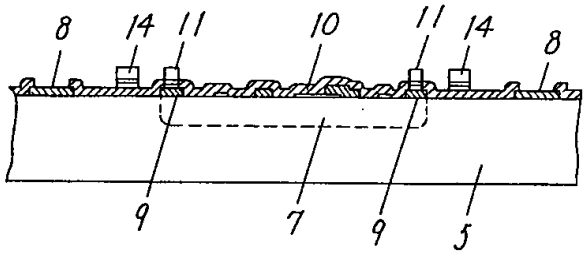
第 1 図



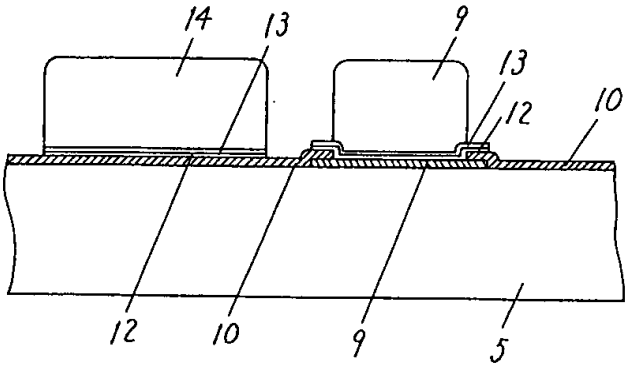

第 2 図



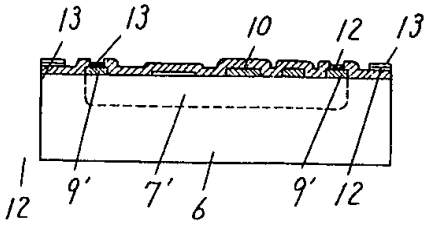

第 3 図




第 4 図



第 5 図




第 6 図